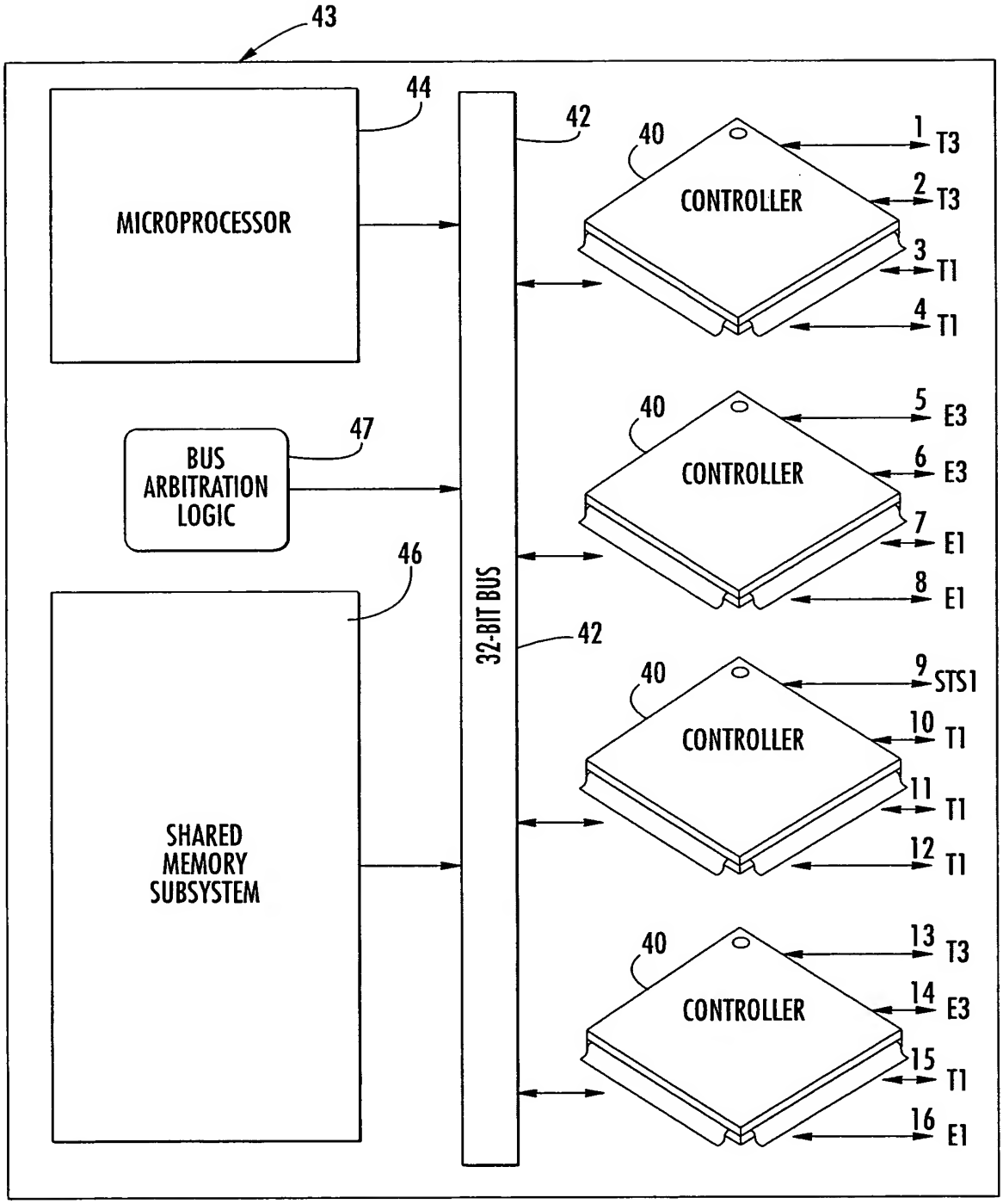
43
44
MICROPROCESSOR
47
BUS ARBITRATION LOGIC
46
SHARED MEMORY SUBSYSTEM
42
32-BIT BUS
42
40
CONTROLLER
1 T3
2 T3
3 T1
4 T1
40
CONTROLLER
5 E3
6 E3
7 E1
8 E1
40
CONTROLLER
9 STS1
10 T1
11 T1
12 T1
40
CONTROLLER
13 T3
14 E3
15 T1
16 E1

FIG. 1

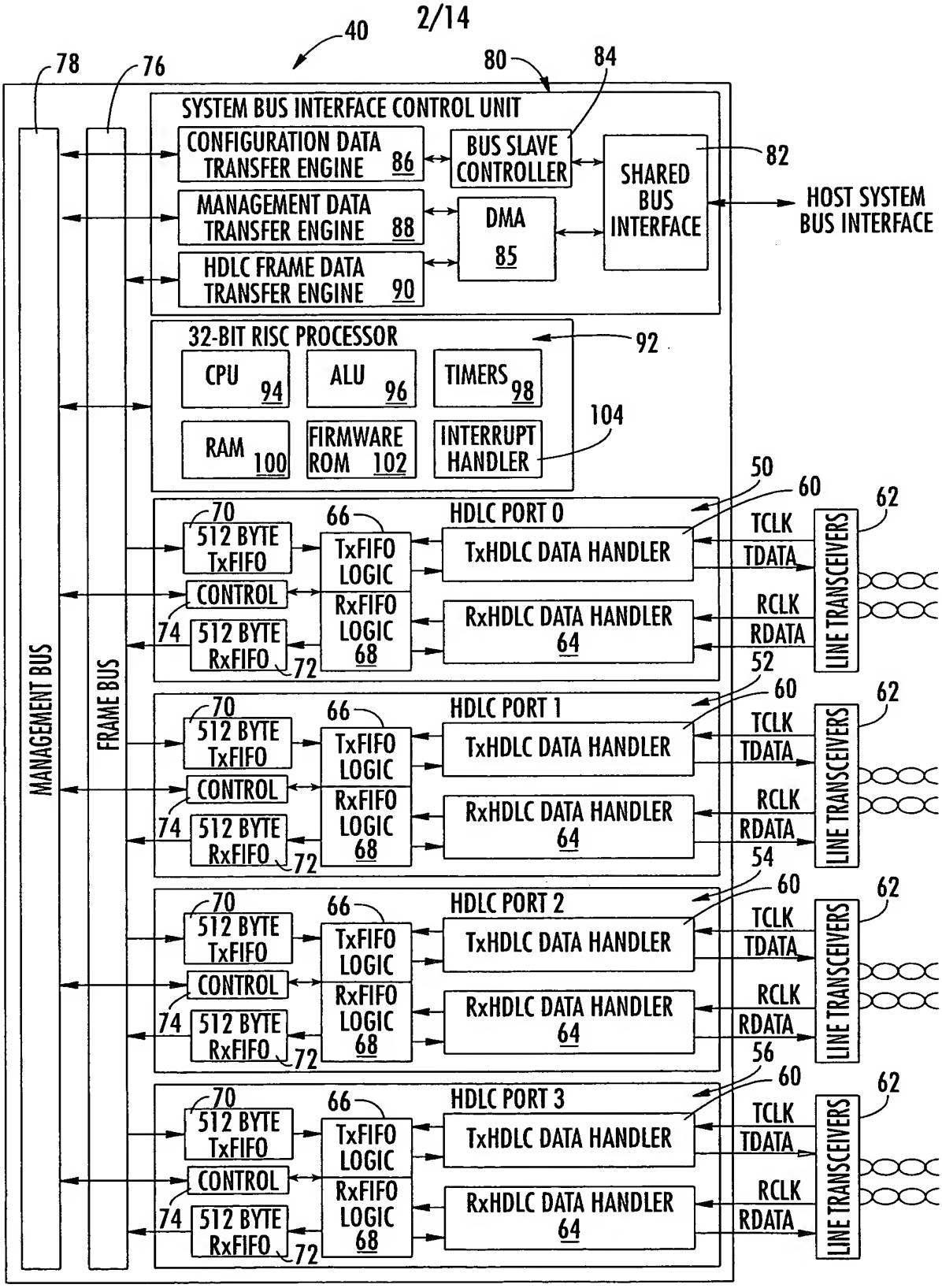
40
78
76
80
84
SYSTEM BUS INTERFACE CONTROL UNIT
CONFIGURATION DATA TRANSFER ENGINE 86
BUS SLAVE CONTROLLER
SHARED BUS INTERFACE
82
HOST SYSTEM BUS INTERFACE
MANAGEMENT DATA TRANSFER ENGINE 88
DMA 85
HDLC FRAME DATA TRANSFER ENGINE 90
32-BIT RISC PROCESSOR
92
CPU 94
ALU 96
TIMERS 98
RAM 100
FIRMWARE ROM 102
INTERRUPT HANDLER
104
MANAGEMENT BUS
FRAME BUS
50
60
62
HDLC PORT 0
70
66
512 BYTE TxFIFO
TxFIFO LOGIC
TxHDLC DATA HANDLER
TCLK
TDATA
CONTROL
RxFIFO LOGIC 68
RxHDLC DATA HANDLER 64
RCLK
RDATA
74
512 BYTE RxFIFO
72
LINE TRANSCEIVERS
52
HDLC PORT 1
54
HDLC PORT 2
56
HDLC PORT 3

FIG. 2

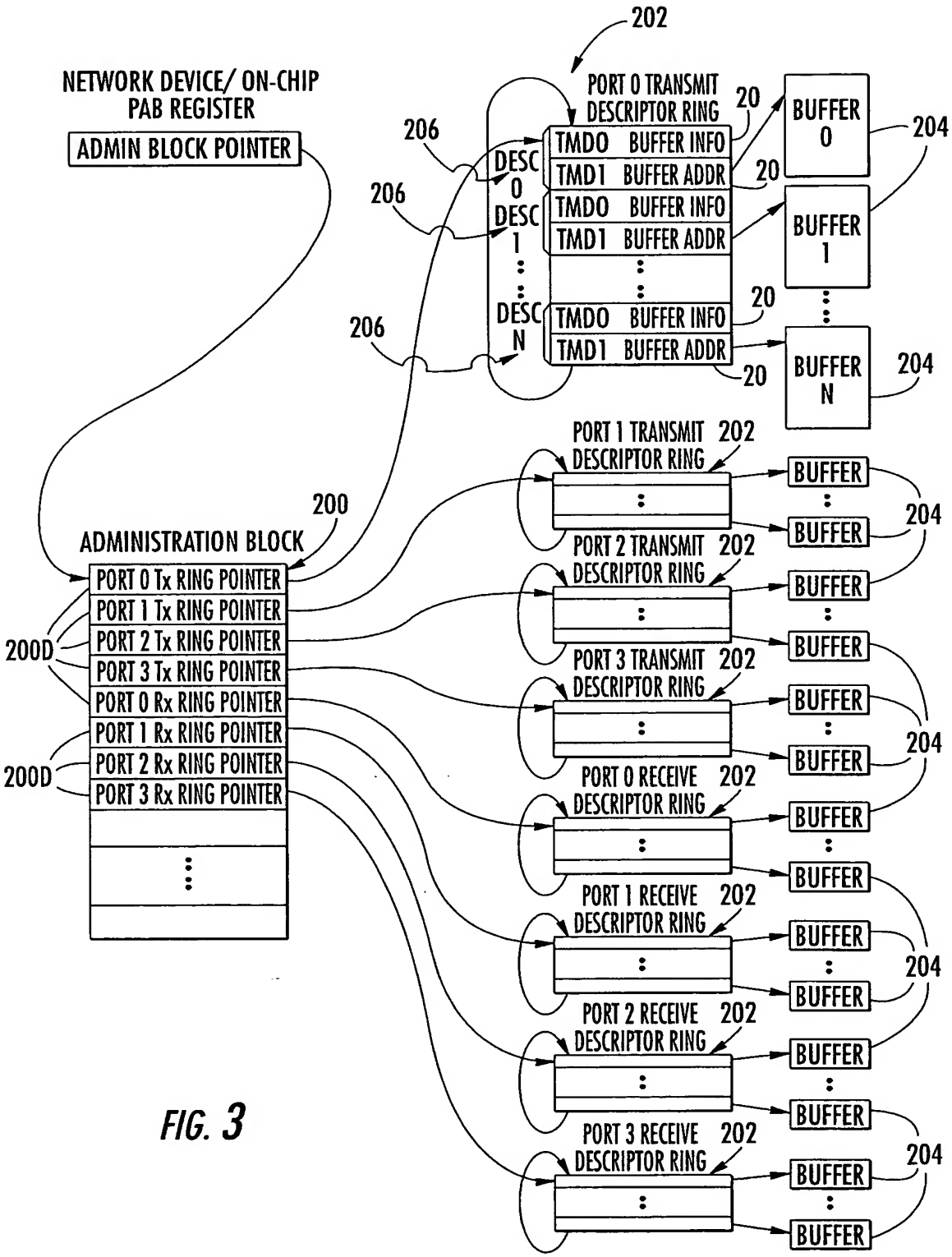
NETWORK DEVICE/ ON-CHIP PAB REGISTER
ADMIN BLOCK POINTER
ADMINISTRATION BLOCK
200
PORT 0 Tx RING POINTER
PORT 1 Tx RING POINTER
PORT 2 Tx RING POINTER
PORT 3 Tx RING POINTER
PORT 0 Rx RING POINTER
PORT 1 Rx RING POINTER
PORT 2 Rx RING POINTER
PORT 3 Rx RING POINTER
200D
200D
202
PORT 0 TRANSMIT DESCRIPTOR RING
206
DESC 0
DESC 1
DESC N
TMD0 BUFFER INFO
TMD1 BUFFER ADDR
20
BUFFER 0
BUFFER 1
BUFFER N
204
PORT 1 TRANSMIT DESCRIPTOR RING
PORT 2 TRANSMIT DESCRIPTOR RING
PORT 3 TRANSMIT DESCRIPTOR RING
PORT 0 RECEIVE DESCRIPTOR RING
PORT 1 RECEIVE DESCRIPTOR RING
PORT 2 RECEIVE DESCRIPTOR RING
PORT 3 RECEIVE DESCRIPTOR RING
BUFFER

FIG. 3

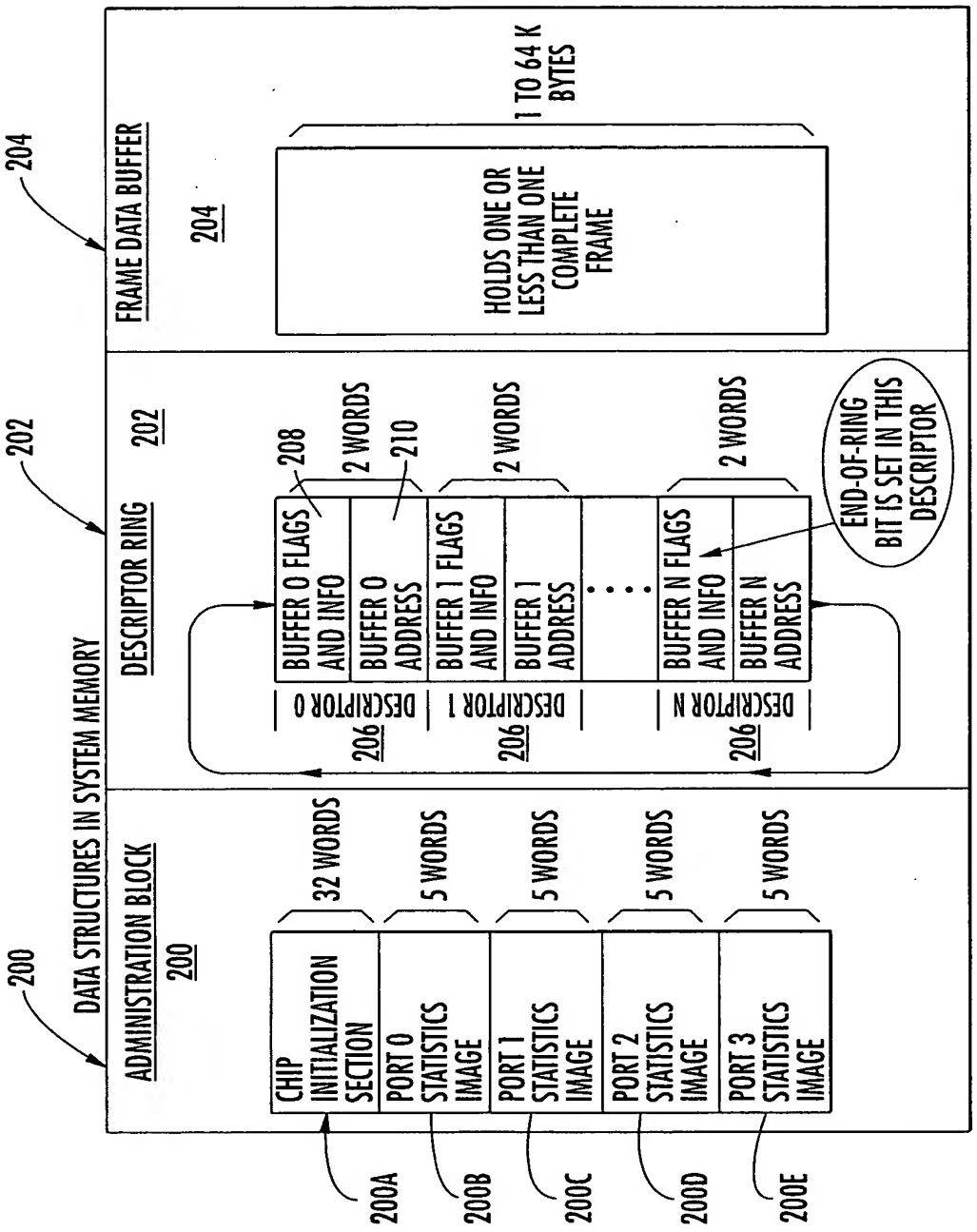
200
DATA STRUCTURES IN SYSTEM MEMORY
ADMINISTRATION BLOCK
200
CHIP INITIALIZATION SECTION
32 WORDS
PORT 0 STATISTICS IMAGE
5 WORDS
PORT 1 STATISTICS IMAGE
5 WORDS
PORT 2 STATISTICS IMAGE
5 WORDS
PORT 3 STATISTICS IMAGE
5 WORDS
200A
200B
200C
200D
200E
202
DESCRIPTOR RING
202
DESCRIPTOR 0
206
BUFFER 0 FLAGS AND INFO
208
BUFFER 0 ADDRESS
210
2 WORDS
DESCRIPTOR 1
206
BUFFER 1 FLAGS AND INFO
BUFFER 1 ADDRESS
2 WORDS
DESCRIPTOR N
206
BUFFER N FLAGS AND INFO
BUFFER N ADDRESS
2 WORDS
END-OF-RING BIT IS SET IN THIS DESCRIPTOR
204
FRAME DATA BUFFER
204
HOLDS ONE OR LESS THAN ONE COMPLETE FRAME
1 TO 64 K BYTES

FIG. 4

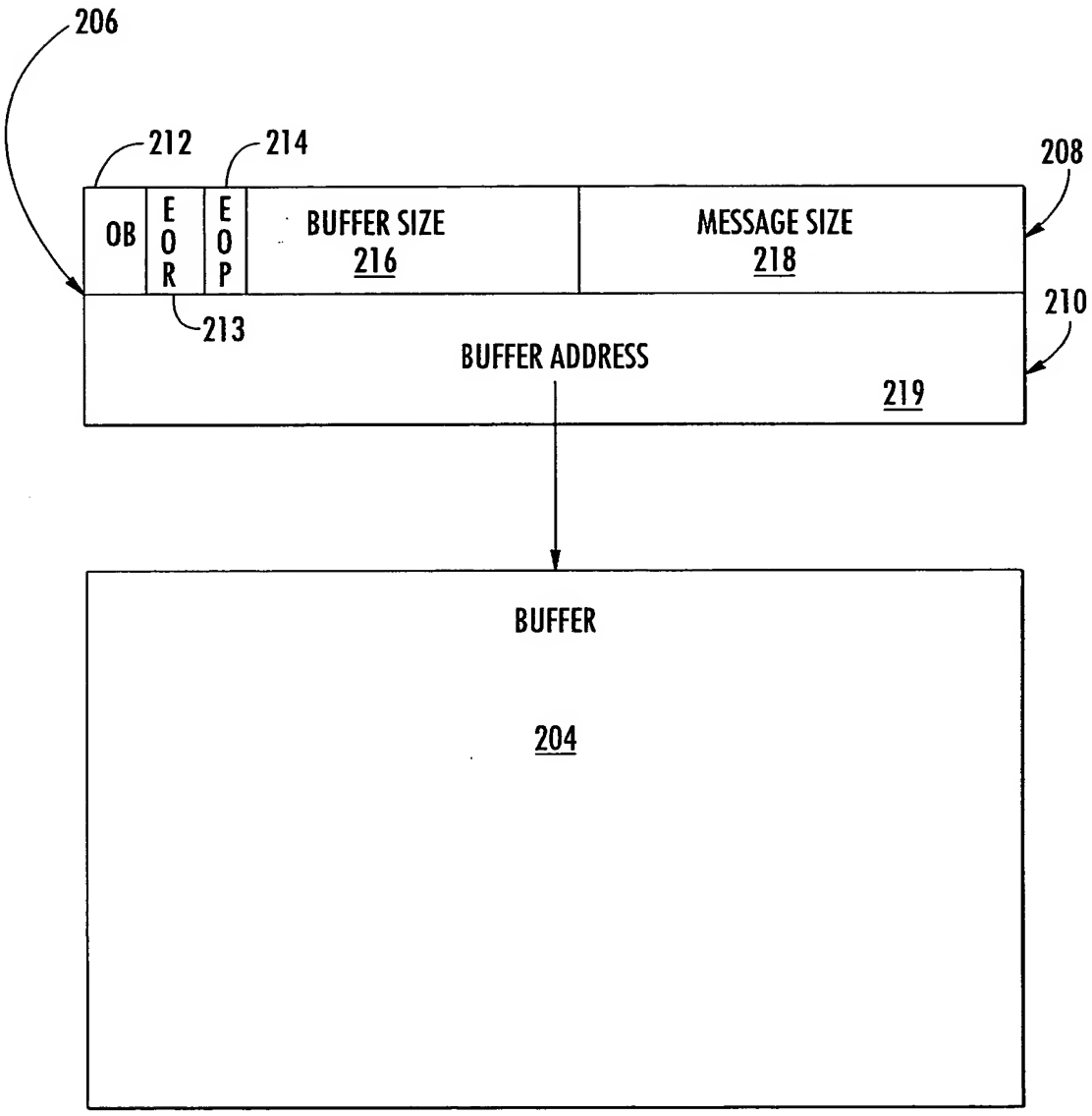
206
212
214
208
OB
E O R
E O P
BUFFER SIZE
216
MESSAGE SIZE
218
210
213
BUFFER ADDRESS
219
BUFFER
204

FIG. 5

FENCEPOST DESCRIPTOR CACHING

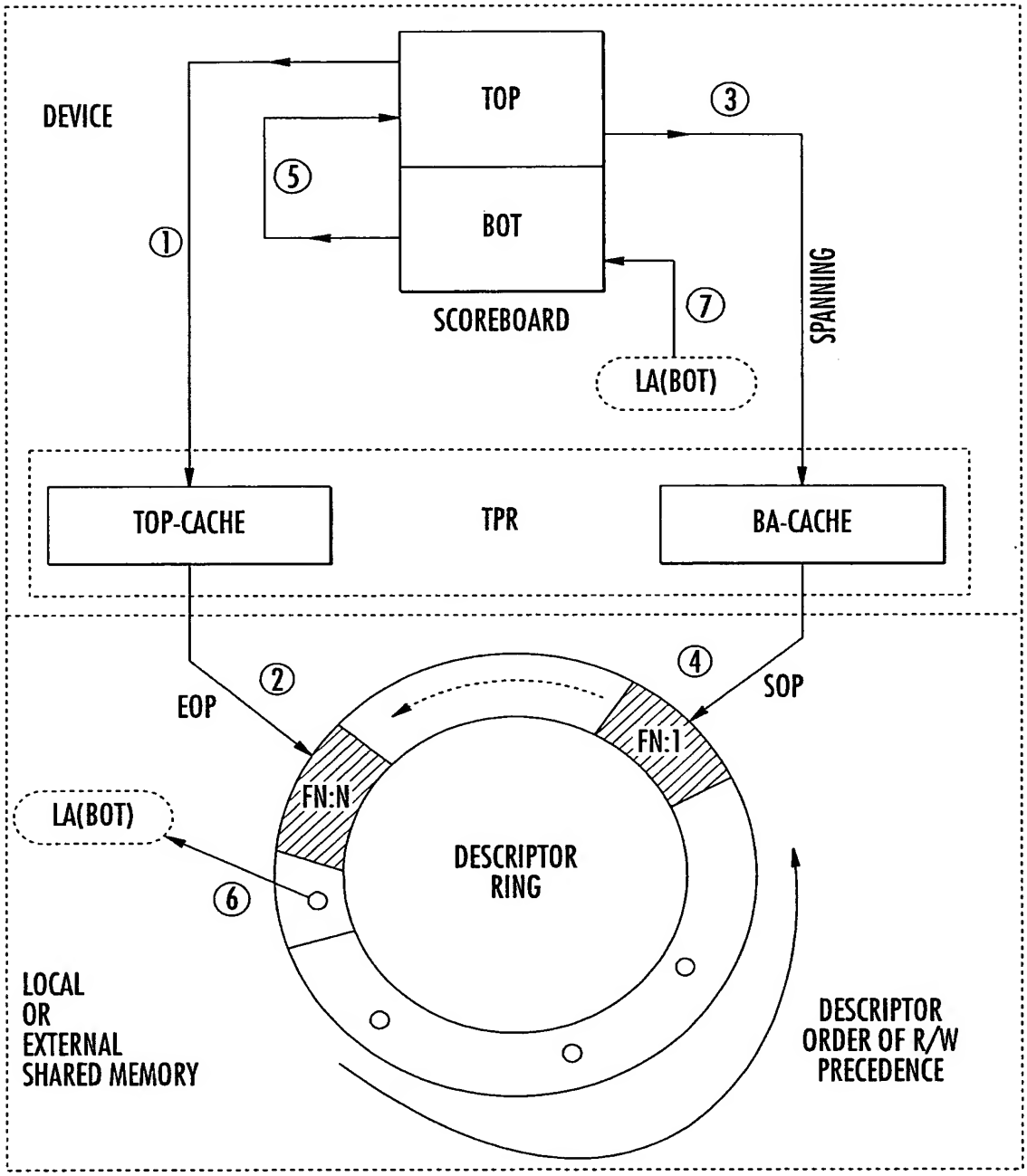

FIG. 6

TPR: SCOREBOARD FORMAT

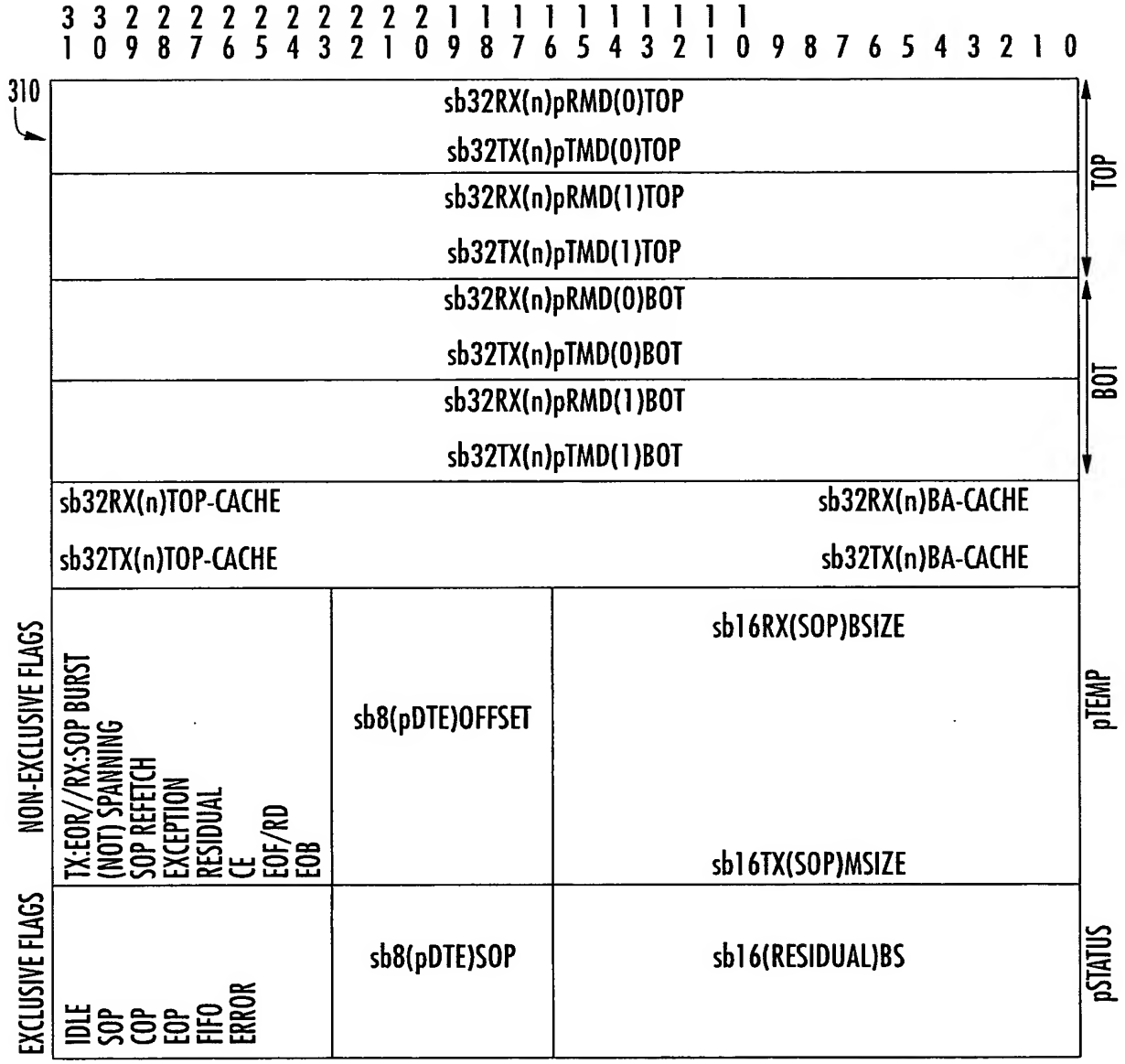

FIG. 7

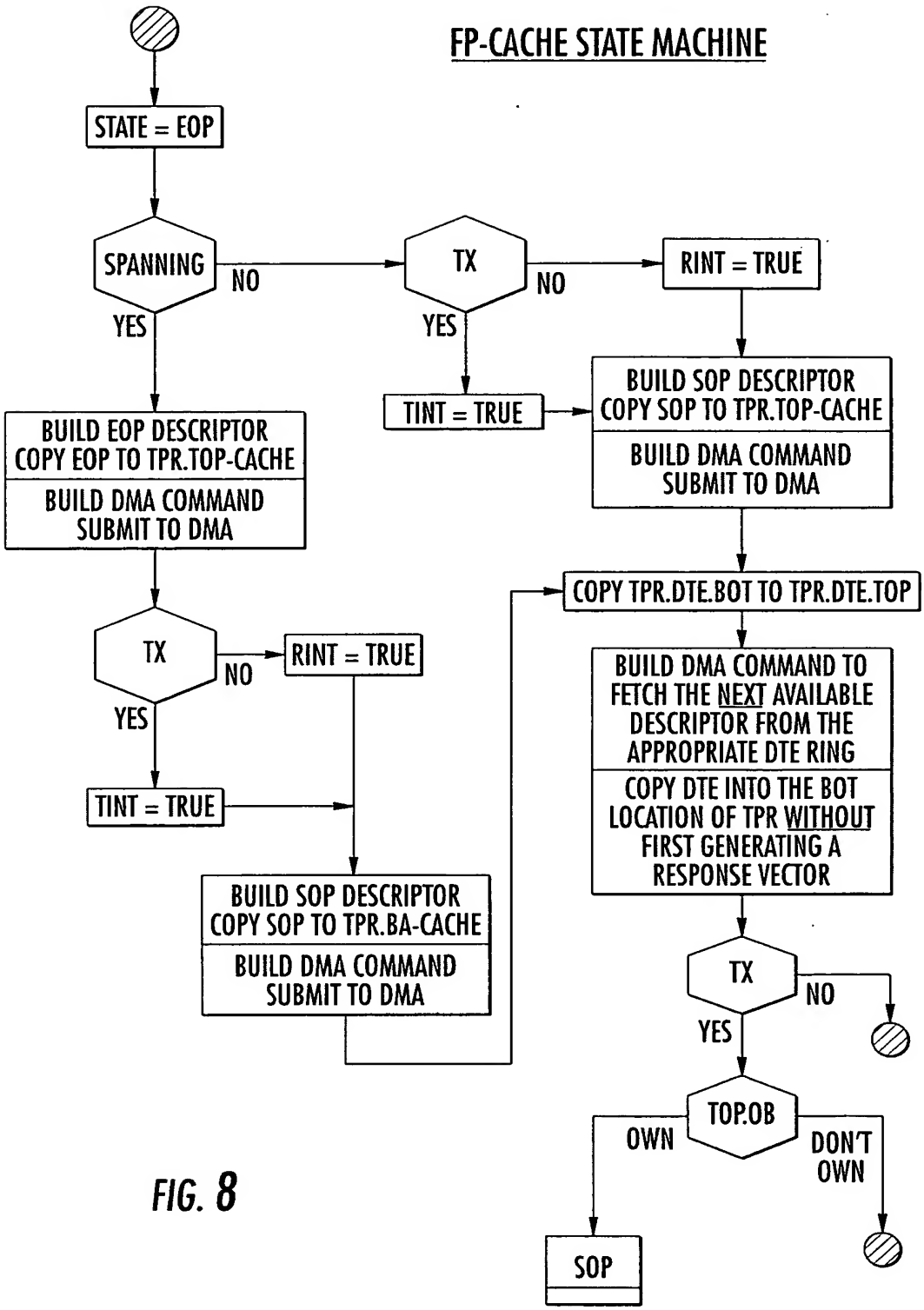
FP-CACHE STATE MACHINE
STATE = EOP
SPANNING
NO
YES
TX
NO
YES
RINT = TRUE
TINT = TRUE
BUILD SOP DESCRIPTOR
COPY SOP TO TPR.TOP-CACHE
BUILD DMA COMMAND
SUBMIT TO DMA
BUILD EOP DESCRIPTOR
COPY EOP TO TPR.TOP-CACHE
BUILD DMA COMMAND
SUBMIT TO DMA
COPY TPR.DTE.BOT TO TPR.DTE.TOP
TX
NO
YES
RINT = TRUE
TINT = TRUE
BUILD DMA COMMAND TO
FETCH THE NEXT AVAILABLE
DESCRIPTOR FROM THE
APPROPRIATE DTE RING
COPY DTE INTO THE BOT
LOCATION OF TPR WITHOUT
FIRST GENERATING A
RESPONSE VECTOR
BUILD SOP DESCRIPTOR
COPY SOP TO TPR.BA-CACHE
BUILD DMA COMMAND
SUBMIT TO DMA
TX
NO
YES
TOP.OB
OWN
DON'T
OWN
SOP

FIG. 8

RECEIVE VS TRANSMIT INTERRUPT STATE MACHINES

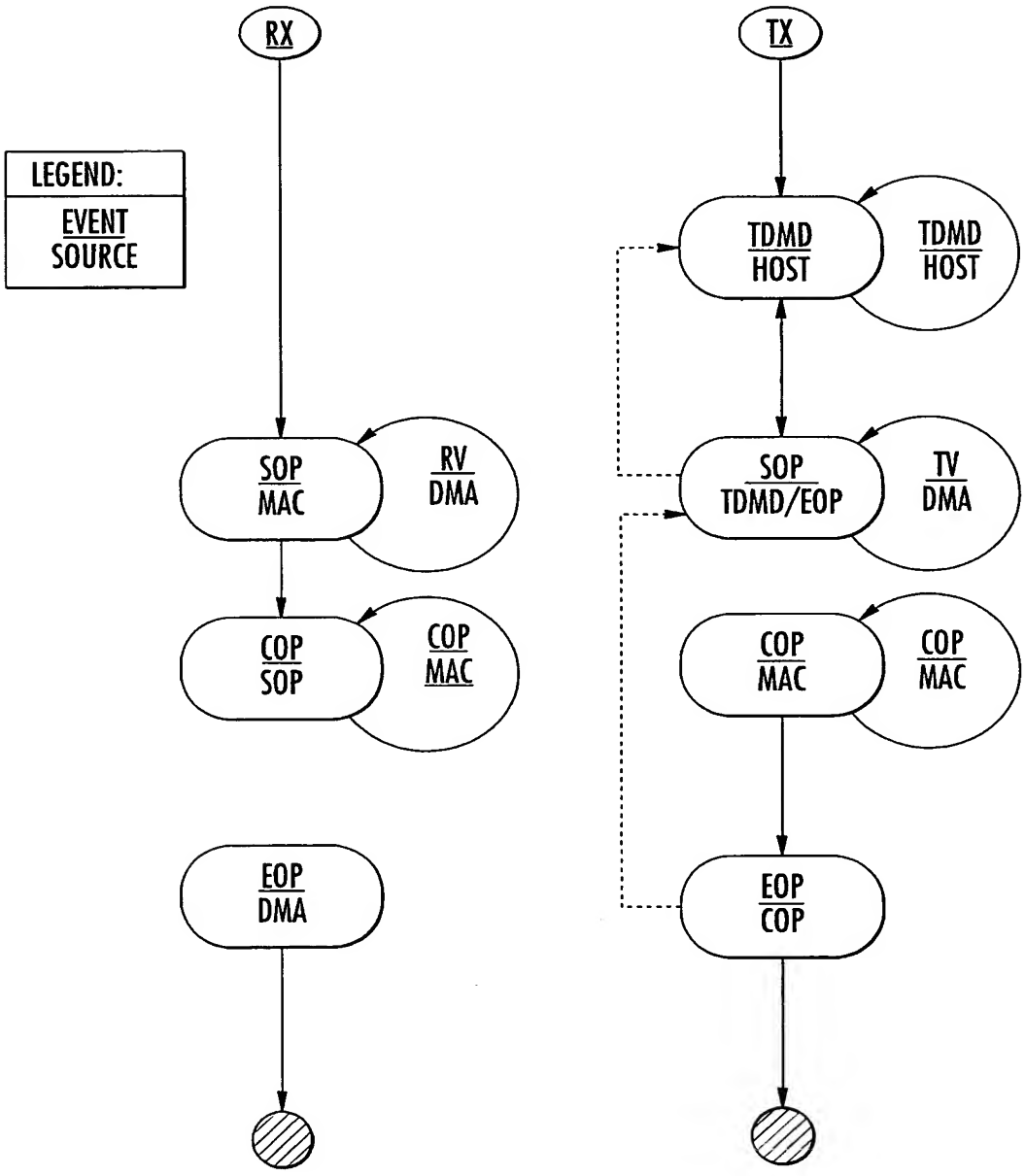

FIG. 9

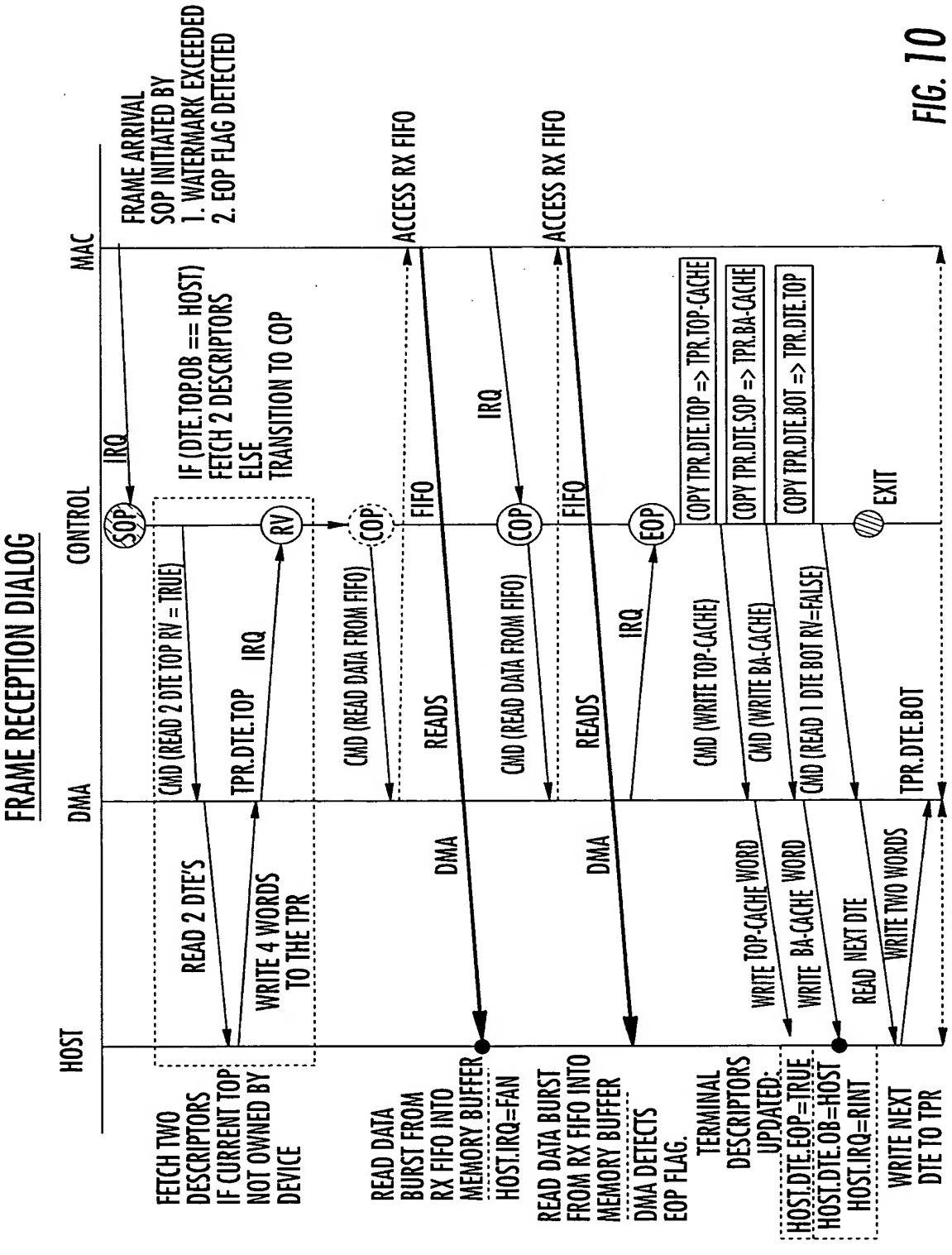
FRAME RECEPTION DIALOG
HOST
DMA
CONTROL
MAC
FRAME ARRIVAL
SOP INITIATED BY
1. WATERMARK EXCEEDED
2. EOP FLAG DETECTED
IRQ
SOP
IF (DTE.TOP.OB == HOST)
FETCH 2 DESCRIPTORS
ELSE
TRANSITION TO COP
CMD (READ 2 DTE TOP RV = TRUE)
READ 2 DTE'S
TPR.DTE.TOP
IRQ
RV
WRITE 4 WORDS
TO THE TPR
COP
CMD (READ DATA FROM FIFO)
ACCESS RX FIFO
FIFO
READS
DMA
IRQ
COP
CMD (READ DATA FROM FIFO)
ACCESS RX FIFO
FIFO
READS
DMA
IRQ
EOP
CMD (WRITE TOP-CACHE)
WRITE TOP-CACHE WORD
CMD (WRITE BA-CACHE)
WRITE BA-CACHE WORD
CMD (READ 1 DTE BOT RV=FALSE)
READ NEXT DTE
WRITE TWO WORDS
TPR.DTE.BOT
(COPY TPR.DTE.TOP => TPR.TOP-CACHE
(COPY TPR.DTE.SOP => TPR.BA-CACHE
(COPY TPR.DTE.BOT => TPR.DTE.TOP
EXIT
INTERNAL BUS
EXTERNAL BUS
FETCH TWO
DESCRIPTORS
IF CURRENT TOP
NOT OWNED BY
DEVICE
READ DATA
BURST FROM
RX FIFO INTO
MEMORY BUFFER
HOST.IRQ=FAN
READ DATA BURST
FROM RX FIFO INTO
MEMORY BUFFER
DMA DETECTS
EOP FLAG.
TERMINAL
DESCRIPTORS
UPDATED:
HOST.DTE.EOP=TRUE
HOST.DTE.OB=HOST
HOST.IRQ=RINT
WRITE NEXT
DTE TO TPR

FIG. 10

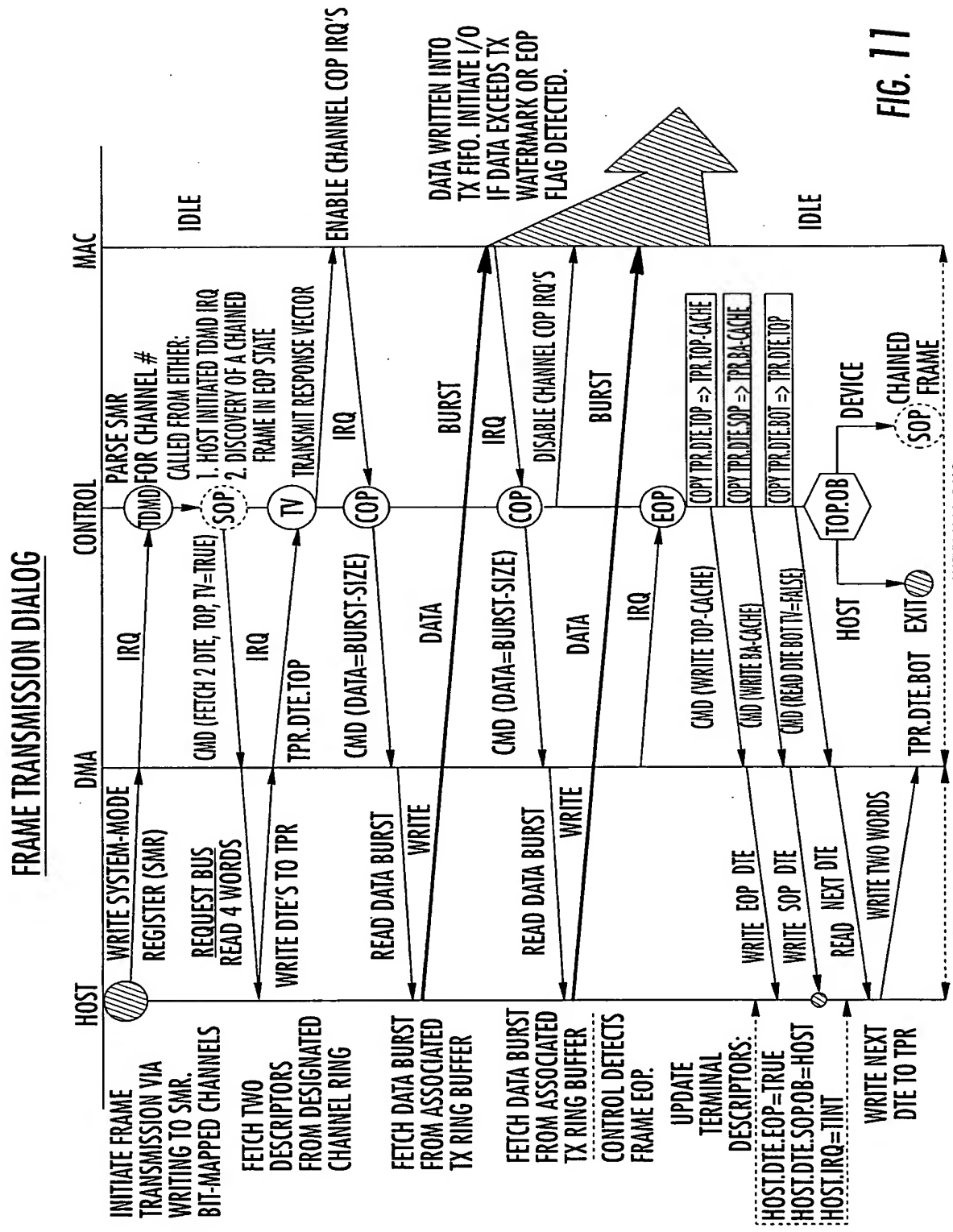
FRAME TRANSMISSION DIALOG
HOST
DMA
CONTROL
MAC
INITIATE FRAME TRANSMISSION VIA WRITING TO SMR. BIT-MAPPED CHANNELS
WRITE SYSTEM-MODE REGISTER (SMR)
IRQ
TDMD
PARSE SMR FOR CHANNEL #
IDLE
FETCH TWO DESCRIPTORS FROM DESIGNATED CHANNEL RING
REQUEST BUS READ 4 WORDS
CMD (FETCH 2 DTE, TOP, TV=TRUE)
SOP
1. HOST INITIATED TDMD IRQ
2. DISCOVERY OF A CHAINED FRAME IN EOP STATE
IRQ
WRITE DTE'S TO TPR
TPR.DTE.TOP
TV
TRANSMIT RESPONSE VECTOR
ENABLE CHANNEL COP IRQ'S
FETCH DATA BURST FROM ASSOCIATED TX RING BUFFER
READ DATA BURST
WRITE
DATA
CMD (DATA=BURST-SIZE)
COP
IRQ
BURST
DATA WRITTEN INTO TX FIFO. INITIATE I/O IF DATA EXCEEDS TX WATERMARK OR EOP FLAG DETECTED.
FETCH DATA BURST FROM ASSOCIATED TX RING BUFFER
READ DATA BURST
WRITE
DATA
CMD (DATA=BURST-SIZE)
COP
IRQ
DISABLE CHANNEL COP IRQ'S
BURST
CONTROL DETECTS FRAME EOP.
IRQ
EOP
UPDATE TERMINAL DESCRIPTORS:
HOST.DTE.EOP=TRUE
HOST.DTE.SOP.OB=HOST
HOST.IRQ=TINT
WRITE EOP DTE
CMD (WRITE TOP-CACHE)
COPY TPR.DTE.TOP => TPR.TOP-CACHE
WRITE SOP DTE
CMD (WRITE BA-CACHE)
COPY TPR.DTE.SOP => TPR.BA-CACHE
READ NEXT DTE
CMD (READ DTE BOT TV=FALSE)
COPY TPR.DTE.BOT => TPR.DTE.TOP
TOP.OB
DEVICE
HOST
CHAINED FRAME
SOP
IDLE
WRITE NEXT DTE TO TPR
WRITE TWO WORDS
TPR.DTE.BOT
EXIT
EXTERNAL BUS
INTERNAL BUS

FIG. 11

[0x31] CMDREG - DMA COMMAND REGISTER

DMA	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT NAME	RESERVED		SFAN	STINT	SRINT	PORT [1:0]		RW	TXERXS	RESDMD	TYPE	NOCRC	RXSEL	REOC	TXEOPA [1:0]		CPC_ADDR[7:0]								XFER_CNT[7:0]							
RESET VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
HOST ACCESS	(READ-ZEROS) / (NO-WRITE)																															
HOST UNLOCK	READ-ONLY																READ-ZEROS/WRITE															
CPC ACCESS	READ-ONLY																READ-ZEROS/WRITE															

BIT #	FIELD	NAME	DESCRIPTION
31:30	RESERVED	--	THESE BITS ARE NOT IMPLEMENTED
29	SFAN	SET FAN	(1=SET: 0=NORMAL) WHEN SET DIRECTS DMA HARDWARE TO GENERATE FAN (BIT 27, 19, 11, 3 OF THE REGISTER MIR) UPON COMPLETION OF THE ASSOCIATED COMMAND TRANSFERING BUFFER OWNERSHIP TO THE HOST. THE DMA SET ONE OF THE FOUR POSSIBLE FAN ACCORDING WITH THE PORT NUMBER SPECIFIED ON THE BITS 26, 25, OF THIS REGISTER.
28	STINT	SET TINT	(1=SET: 0=NORMAL) WHEN SET DIRECTS DMA HARDWARE TO GENERATE TINT (BIT 25, 17, 9, 1 OF THE REGISTER MIR) UPON COMPLETION OF THE ASSOCIATED COMMAND TRANSFERING BUFFER OWNERSHIP TO THE HOST. THE DMA SET ONE OF THE FOUR POSSIBLE TINT ACCORDING WITH THE PORT NUMBER SPECIFIED ON THE BITS 26, 25, OF THIS REGISTER.
27	SRINT	SET RINT	(1=SET: 0=NORMAL) WHEN SET DIRECTS DMA HARDWARE TO GENERATE RINT (BIT 24, 16, 8, 0 OF THE REGISTER MIR) UPON COMPLETION OF THE ASSOCIATED COMMAND TRANSFERING BUFFER OWNERSHIP TO THE HOST. THE DMA SET ONE OF THE FOUR POSSIBLE TINT ACCORDING WITH THE PORT NUMBER SPECIFIED ON THE BITS 26, 25, OF THIS REGISTER.
26:25	PORT	PORT NUMBER	(11=PORT 3; 10=PORT 2; 01=PORT 1; 00=PORT 0) *ONLY FOR FIFO/SYSMEM TRANSFERS.* INDICATES THE HDLC PORT NUMBER TO BE USED BY THE DMA FOR FIFO/SYSMEM TRANSFER.
24	RW	SYSTEM MEMORY READ/WRITE	(1=READ: 0=WRITE) *USED FOR ALL TRANSFER TYPES.* INDICATES THE DIRECTION OF DATA FLOW WITH RESPECT TO SYSTEM MEMORY. WHEN USED FOR FIFO/SYSMEM TRANSFERS THIS FIELD CAN ALSO BE THOUGHT OF AS SELECTING THE Tx- OR Rx-FIFO WITHIN THE HDLC PORT INDICATED IN THE PORT FIELD (Tx=1; Rx=0).
23	TXERXS	Tx END-OF FRAME/ Rx START-OF-FRAME	(1=Tx EOP OR Rx SOP; 0=NORMAL) *ONLY USED FOR FIFO/SYSMEM TRANSFERS.* SYSMEM-TO-FIFO TRANSFERS (RW=1): INDICATES THIS COMMAND CONSTITUTES THE FINAL TRANSFER OF DATA FOR A GIVEN TRANSMIT FRAME. FIFO-TO-SYSMEM TRANSFERS (RW=0): INDICATES THIS COMMAND IS THE FIRST DATA TRANSFER FOR A GIVEN RECEIVE FRAME.
22	RESDMD	RESPONSE DEMAND	(1=GENERATE RESPONSE; 0=NO RESPONSE) *USED FOR ALL TRANSFER TYPES.* ALLOWS THE FIRMWARE TO CONTROL WHETHER OR NOT AN INTERRUPT WILL BE GENERATED FOR THIS COMMAND BY THE DMA. WHEN THIS BIT IS SET THE DMA WILL GENERATES ONE OF THE 8 POSSIBLE INTERRUPTS. EACH INTERRUPT IS RELATIVE TO ONE OF THE 4 PORTS, ACCORDING TO THE PORT NUMBER SPECIFIED ON THE BITS 26,25, AND THE DIRECTION OF THE DATA FLOW SPECIFIED ON THE BIT 24 OF THIS REGISTER.
21	TYPE	TRANSFER TYPE	(1=TPR/SYSMEM TRANSFER; 0=FIFO/SYSMEM TRANSFER) *USED FOR ALL TRANSFER TYPES.* DETERMINES WHETHER THE DMA WILL PERFORM A TPR/SYSMEM TRANSFER OR A FIFO/SYSMEM TRANSFER.

FIG. 12A

BIT #	FIELD	NAME	DESCRIPTION
20	NOCRC	NO Tx CRC	(1=CRC NOT APPENDED; 0=CRC APPENDED) *ONLY FOR SYSMEM-TO-FIFO TRANSFERS WHEN RW=1 AND TXERXS=1.* ALLOWS THE FIRMWARE TO CONTROL WHETHER OR NOT THE HDLC TRANSMITTER WILL APPEND A CRC TO THE END OF A GIVEN TRANSMIT FRAME.
19	RXSEL	Rx SELECTION	(1=RX; 0=TX) THIS BIT DISTINGUISH BETWEEN GENERATIN THE RX OR THE TX RESPONSE DEMAND INTERRUPT.
18	REOC	REQUEST END OF COMMAND	(1=SET; 0=NORMAL) WHEN SET DIRECTS DMA HARDWARE TO SET THE BIT 3 OF THE DMASTAT AFTER COMPLETION OF THE CURRENT COMMAND.
17:16	TXEOPA	TRANSMIT END-OF-FRAME ALIGNMENT	(11=3 BYTE; 10=2 BYTES; 01=1 BYTE; 00=4 BYTES) *ONLY FOR SYSMEM-TO-FIFO TRANSFERS WHEN RW=1 AND TXERXS=1.* COMMUNICATES TO THE DMA THE NUMBER OF VALID BYTES IN THE LAST WORD OF A TRANSMIT FRAME TRANSFER.
15:8	CPC_ADDR	CPC ADDRESS	(8-BIT BINARY VALUE) *ONLY FOR TPR/SYSMEM TRANSFERS.* INDICATES THE STARTING WORD ADDRESS WITHIN THE CPC'S MEMORY. THE DMA HAS NO PROVISION TO PROTECT FROM WRAP-AROUND (0xFF TO 0x00).
7:0	XFER_CNT	TRANSFER COUNT	(8-BIT BINARY VALUE) *USED FOR ALL TRANSFER TYPES.* INDICATES THE FIRMWARE-REQUESTED NUMBER OF DATA-TRANSFERRING UCLK CYCLES THE DMA WILL PERFORM – KNOWN AS THE "BURST SIZE". THIS IS THE NUMBER 4-BYTE WORDS THE DMA WILL TRANSFER DURING ITS EXECUTION OF THE COMMAND. EXCEPTIONS OCCURE WHEN THE DMA ENCOUNTERS Rx END-OF-FRAME BEFORE THE TRANSFER COUNT HAS BEEN SATISFIED AND/OR WHEN ONE OR MORE OF THE BYTES WITHIN A WORD BEING TRANSFERRED ARE NOT VALID (INDICATED BY THE DBYTE(3:0) PINS). A VALUE OF 0x00 INDICATES A BURST SIZE OF 256.

FIG. 12B

FIGURE DMA COMMAND QUEUE ILLUSTRATION

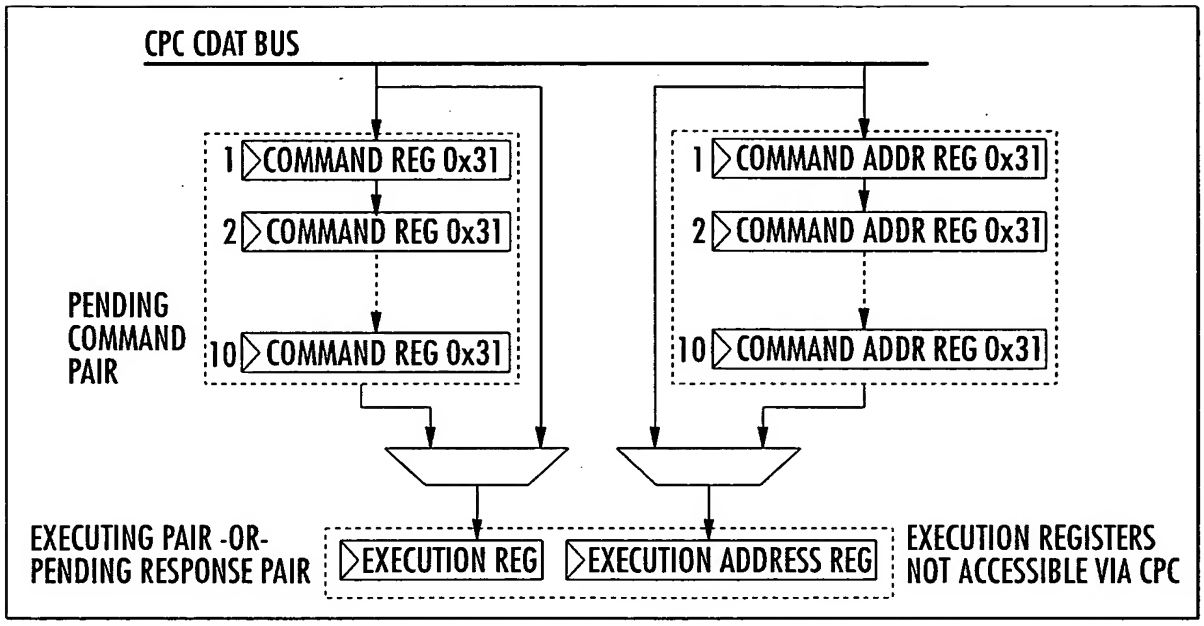

FIG. 13